

Q11
concl'd

-one or more dielectric layers comprised of latex; and
-one or more layers of electrically conductive material
patterned to form multiple electrical interconnects,
with each such electrically conductive layer placed on
top of one of said dielectric layers.

Please cancel claims 14 through 16.

Please amend Claim 17 to read as follows:

- 17. (Amended) A multichip module comprising:
- a plurality of integrated circuits mounted on a substrate;
 - one or more flexible dielectric layers comprised of latex; and
 - one or more layers of electrically conductive material patterned to form multiple electrical interconnects between bonding pads on different ones of said integrated circuits, with each such electrically ~~conductive layer~~ **conductive material layer** placed on top of one of said dielectric layers.

Q12

B

Please cancel Claims 18 through 22.

Please add new claims 45 through 54 as follows:

- 45. A circuit as in Claim 11 wherein:
- one or more of said latex layers has a top surface that contains peaks and valleys of a size that would not occur on the top surface of the latex had it not been roughened, and

Q13

B

electrically material

-one or more of said ^{electrically}conductive ^{material}layers is formed of a first conductive metal that substantially fills said valleys formed in the portion of the latex layer's top surface over which the conductive layer's metal has been patterned, so as to increase the ability of said metal to adhere to said latex surface.

-46. A circuit as in Claim 45 wherein the portions of said one or more layers of the first conductive metal adjacent said latex layer between said peaks and valleys contain particles of a second metal that were used as catalytic seed particles to promote the deposition of said first metal onto the roughened top surface of said latex layer.

-47. A circuit as in Claim 46 wherein a majority of the catalytic seed particles contained in said first conductive metal adjacent the top surface of said latex layer contain only two to six atoms of said second metal.

-48. A circuit as in Claim 46 wherein the second metal of which said catalytic seed particles are formed is a metal in the eighth group of the periodic table.

-49. A circuit as in Claim 46 wherein said second metal is palladium.

-50. A multichip module as in Claim 17 wherein:

-one or more of said latex layers has a top surface that contains peaks and valleys of a size that would not occur on the top surface of the latex had it not been roughened, and

B

electrically material
-one or more of said conductive layers is formed of a first conductive metal that substantially fills said valleys formed in the portion of the latex layer's top surface over which the conductive layer's metal has been patterned, so as to increase the ability of said metal to adhere to said latex surface.

Q13
concl'd
-51. A multichip module as in Claim 50 wherein the portions of said one or more layers of the first conductive metal adjacent said latex layer between said peaks and valleys contain particles of a second metal that were used as catalytic seed particles to promote the deposition of said first metal onto the roughened top surface of said latex layer.

-52. A multichip module as in Claim 51 wherein a majority of the catalytic seed particles contained in said first conductive metal adjacent the top surface of said latex layer contain only two to six atoms of said second metal.

-53. A multichip module as in Claim 51 wherein the second metal of which said catalytic seed particles are formed is a metal in the eighth group of the periodic table.

-54. A multichip module as in Claim 52 wherein said second metal is palladium.
